6-22-05

2128

Atty Docket No. 003921.00011

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:

Terry Lee GOODE

U.S. Pat. App. No.: 09/841,974

Filing Date: April 24, 2001

For: EMULATOR WITH SWITCHING NETWORK CONNECTIONS

Examiner: Fred O. Ferris, III

Group Art Unit: 2128

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Alexandria, Virginia 22313-1450

Sir:

Pursuant to his duty of disclosure under 37 C.F.R. §1.56, Applicant brings the documents listed in the attached PTO-1449 form to the attention of the Examiner in the above-identified patent application.

In accordance with the Notice published in the Official Gazette of August 5, 2003, Applicant has not provided copies of the U.S. patents and published U.S. patent applications listed in the attached PTO-1449. A copy of each of the listed foreign patent documents and non-patent literature, however, is attached hereto.

A first Official Action issued for this application on November 9, 2004. Accordingly, the Commissioner is authorized to charge the fee required under 37 C.F.R. §1.97(c)(2) to Deposit Account No. 19-0733. Applicant therefore submits that this Information Disclosure Statement is being timely presented in accordance with 37 C.F.R. §1.97(c).

While Applicant is presenting the documents listed in the attached PTO-1449 form, Applicant does not waive any right to take appropriate action to establish patentability over the listed documents should one or more of these documents be applied as a reference against any claim in this application.

Applicant respectfully asks that the documents listed on the attached PTO-1449 form be considered by the Examiner and made officially of record, and that a listing of the same appear on the face of any patent which may issue from this application.

Respectfully submitted,

Banner & Witcoff, Ltd.
1001 G Street, N.W., 11th Floor
Washington, D.C. 20001-4597
Telephone: (202) 824-3000
Facsimile: (202) 824-3001
June 20, 2005

By: Thomas L. Evans
Thomas L. Evans, Reg. No. 35,805

PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete If Known	
Application Number	09/841,974
Filing Date	4/24/01
First Named Inventor	Terry Lee Goode
Art Unit	2128
Examiner Name	Fred O. Ferris III
Attorney Docket Number	003921.00011

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,649,176	07-15-1997	Selvidge, et al.	
		US- 5,659,716	08-19-1997	Selvidge, et al.	
		US- 5,841,967	11-24-1998	Sample, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP 1-154251	06-1989			No
		GB 1,444,084	07-28-1976	Cheesman		
		GB 2,182,220	05-07-1987	Austin		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08b(08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	09/841,974
Filing Date	4/24/01
First Named Inventor	Terry Lee Goode
Art Unit	2128
Examiner Name	Fred O. Ferris III
Attorney Docket Number	003921.00011

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		Kronstadt, et al., "Software Support for the Yorktown Simulation Engine," 19th Design Automation Conference, Paper 7.3, 1982, pp. 60-64	
		Koike, et al., "HAL: A High-Speed Logic Simulation Machine," IEEE Design & Test, Oct. 1985, pp. 61-73	
		Shear, "Tools Help you Retain the Advantages of Using Breadboards in Gate-Array Design," EDN, Mar. 18, 1987, pp. 81-88	
		J.W. Babb, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation," Masters Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, Nov. 1993; Also available as MIT/LCS Technical Report TR-686	
		M. Dahl, J. Babb, R. Tessier, S. Hanono, D. Hoki, and A. Agarwal, "Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation System, " IEEE Workshop on FPGAs for Custom Computing Machines '94 (FCCM '94), Apr. 1994	
		R. Tessier, J. Babb, M. Dahl, D. Hanono and A. Agarwal, "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment," ACM Workshop on FPGA's (FPGA '94), Feb. 1994	
		J. Babb, R. Tessier, and A. Agarwal, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," IEEE Workshop on FPGAs for Custom Computing Machines '93 (FCCM '93), Apr. 1993	
		IKOS Systems to Acquire Virtual Machine Works; IKOS Systems Mar. 11, 1996	
		R. Goering, "Emulation for the Masses," Electronic Engineering Times, Jan. 1996	
		J. Babb, R. Tessier, and A. Agarwal, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," Massachusetts Institute of Technology, Student Workshop on Scalable Computing, August 4, 1993	
		R. Tessier, J. Babb, M. Dahl, D. Hanono, and D. Hoki, 'The Virtual Wires Emulation System; A Gate-Efficient ASIC Prototyping Environment," MIT Student Workshop on Scalable Computing; July 21-22, 1994	
		Feng, "A Survey of Interconnection Networks," Computer, Dec. 1981, pp. 12-27	
		Chapter 36, "Switching Networks and Traffic Concepts," Reference Data for Radio Engineers, Howard W. Sams & Co., 1981, pp. 36-1 to 36-16	
		S. Hanono, "Inner View Hardware Debugger: A Logic Analysis Tool for the Virtual Wires Emulation System," Masters Thesis, MIT Department of Electrical Engineering and Computer Science, Jan. 1995; Also available as MIT/LCS Technical Report.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.